# ADSP-21367/8/9 DATASHEET CHANGES

**SET-1:** The $t_{DDTE}$ & $t_{SDRE}$ specs for 400MHz and 333MHz parts are tightened to help ease board design requirements for the customers. The $t_{DDTE}$ spec for 266MHz has been marginally relaxed with negligible impact on customer designs.

| Spec Name | Interface | From (rev C Datasheet) | To (rev D datasheet) | Table # |
|---|---|---|---|---|
| $t_{DDTE}$ (400MHz) | Serial port Ext Clk | 9.6 | 7.8 | Table 29 |
| $t_{DDTE}$ (266MHz) | Serial port Ext Clk | 9.6 | 9.8 | Table 29 |
| $t_{SDRE}$ (400MHz) | Serial port Ext Clk | 2.5 | 1.9 | Table 29 |
| $t_{SDRE}$ (333MHz) | Serial port Ext Clk | 2.5 | 2.0 | Table 29 |

**SET-2:** The following specs are changed from fixed value to equation based so that they scale better with the core frequency.

| Spec Name | Interface | From (ns) | To (ns) | Table # |
|---|---|---|---|---|
| $t_{IDPCLK}$ | Input Data port | 20 | tCCLK*8 | Table 33 |
| $t_{IDPCLKW}$ | Input Data port | 9 | (tCCLK*8)/2 -1 | Table 33 |
| $t_{PDCLK}$ | PDAP | 20 | tCCLK*8 | Table 34 |
| $t_{PDCLKW}$ | PDAP | 7 | (tCCLK*8)/2 -3 | Table 34 |
| $t_{SRCCLKW}$ | SRC serial input and output port | 9 | (tCCLK*8)/2 -1 | Tables 36 and 37 |
| $t_{SRCCLK}$ | SRC serial input and output port | 20 | tCCLK*8 | Tables 36 and 37 |
| $t_{SCLKW}$ | Serial port Ext Clk | 10 | (tCCLK*8)/2  - 0.5 | Table 29 |
| $t_{SCLK}$ | Serial port Ext Clk | 20 | tCCLK*8 | Table 29 |

**ANALOG DEVICES**